SA51

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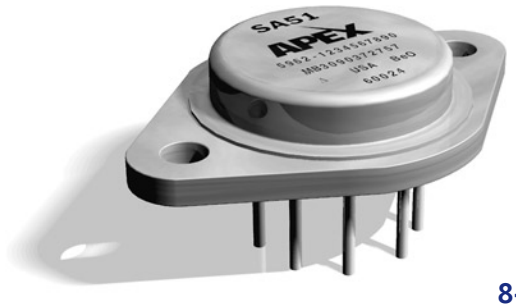
FEATURES

- LOW COST COMPLETE H-BRIDGE
- SELF-CONTAINED SMART LOWSIDE/HIGHSIDE DRIVE CIRCUITRY
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE: UP TO 80V
- 5A CONTINUOUS OUTPUT
- HERMETIC SEALED PACKAGE
- HIGH EFFICIENCY: 95%
- FOUR QUADRANT OPERATION, TORQUE CONTROL CAPABILITY



8-PIN TO-3
PACKAGE STYLE CE

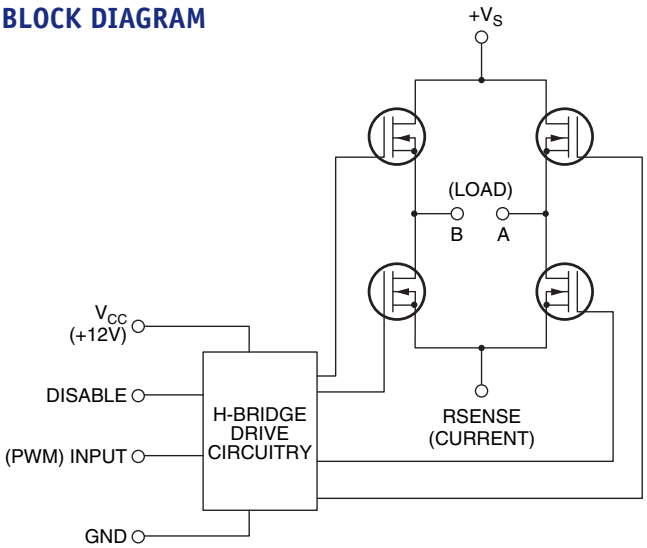
APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- CLASS D SWITCHMODE AMPLIFIER
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

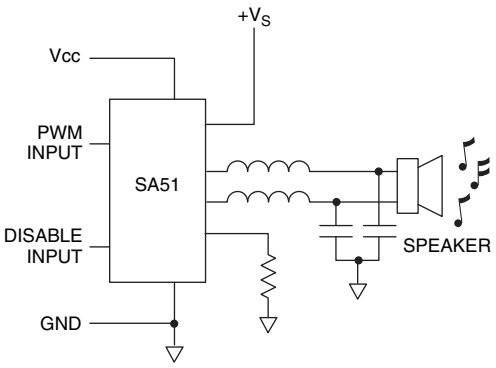
DESCRIPTION

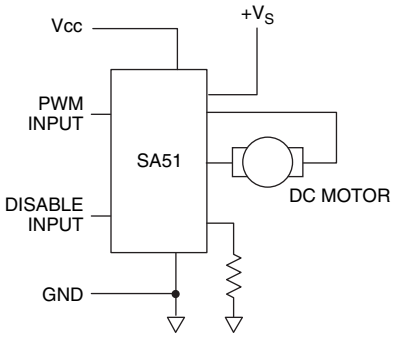
The SA51 is a pulse width modulation amplifier that can supply 5A continuous current to the load. The full bridge amplifier can be operated over a wide range of supply voltages. All of the drive/control circuitry for the lowside and highside switches are internal to the hybrid. The user provides a TTL compatible PWM signal for simultaneous amplitude and direction control in four quadrant mode. The internal circuitry will provide proper deadtime protection for each half bridge. All N-channel FETs mean the best efficiency for the size, both in terms of on-resistance and switching capability. For an idle/sleep mode or for fault protection, a TTL compatible disable pin is provided so as to shut down all four transistors. The SA51 is packaged in a space efficient isolated 8-pin TO-3 that can be directly connected to a heatsink.

BLOCK DIAGRAM

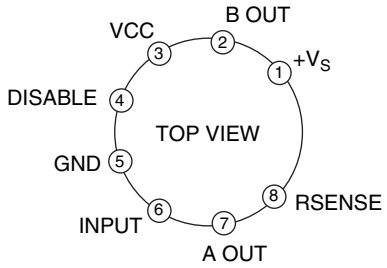


TYPICAL APPLICATION





EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	80V[5]
OUTPUT CURRENT, peak	7A
LOGIC SUPPLY VOLTAGE, Vcc	16V
POWER DISSIPATION, internal	120W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[3]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–65 to +125°C
INPUT VOLTAGE, INPUT	0 to Vcc
INPUT VOLTAGE, DIS	0 to Vcc

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
PWM PULSE LOW VOLTAGE		0		0.6	Vdc
PWM PULSE HIGH VOLTAGE		3.6		5.0	Vdc
PWM FREQUENCY			45	500	KHz
DISABLE ON		3.6		V_{CC}	Vdc
DISABLE OFF		0		0.6	Vdc
OUTPUT					
Vds (ON) VOLTAGE, each MOSFET	Ids = 5A		1.25	1.8	Vdc
TOTAL Ron, both MOSFETs			0.5		Ω
EFFICIENCY, 5A OUTPUT	$+V_S$ = 80V		95		%
CURRENT, continuous		5			A
CURRENT, peak	T = 100ms	7			A
SWITCHING CHARACTERISTICS[4]	$+V_S$ = 28V, Vcc = 12V, Ic =2A				
RISE TIME			36	54	nS
FALL TIME			170	250	nS
DEAD TIME			100		nS
POWER SUPPLY					
$+V_S$ VOLTAGE[5]	$+V_S$ Current = Load Current			80	Vdc
Vcc VOLTAGE		9.5	12	15	Vdc
Vcc CURRENT	Vcc = 12Vdc		11	18	mA
THERMAL[3]					
RESISTANCE, junction to case	Full temp range, for each transistor		2.0		°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case		–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 60W.
2. Unless otherwise noted: T_C = 25°C, Vcc = 12Vdc.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. Derate to 70V below T_C = +25°C.

CAUTION

The SA51 is constructed from MOSFET transistors. ESD handling procedures must be observed.

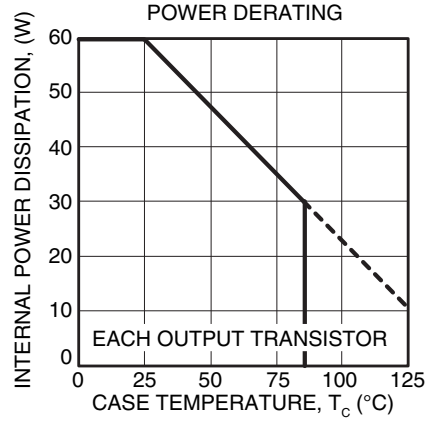
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

WARNING—AMPLIFIER PROTECTION

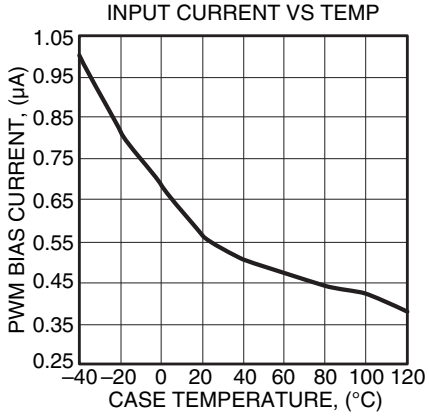
The SA51 contains an internal logic chip that turns on and turns off output MOSFET drivers at a certain sequence. Noise or oscillation caused by external wiring inductance, lack of proper power supply bypass capacitors, ground, supply, and local internal loops may be fed back to this logic chip and cause it to turn on one or more MOSFET drivers at the wrong time, thus destroying the SA51. **A well laid out PC board with low impedance copper ground plane is necessary for the SA51 to function properly.** The Apex EK-SA51 evaluation board is recommended for fast and easy breadboarding of circuits using the SA51.

Typical performance curves with Vcc = 12V, PWM at 45kHZ and case temperature at 25°C, unless otherwise specified.

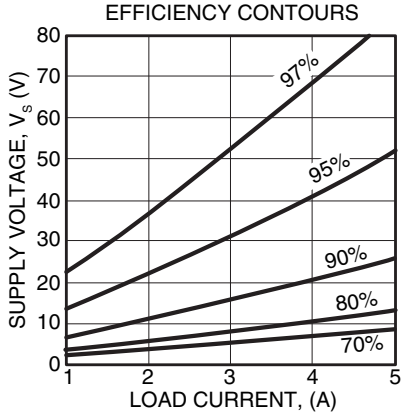
POWER DERATING



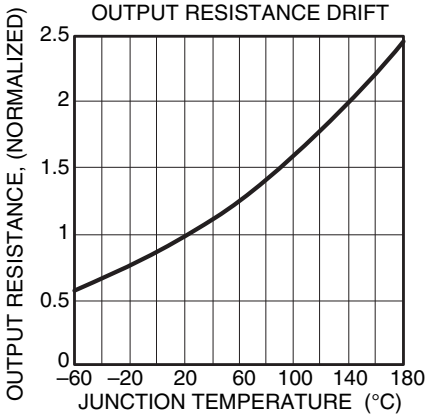
INPUT CURRENT VS TEMP



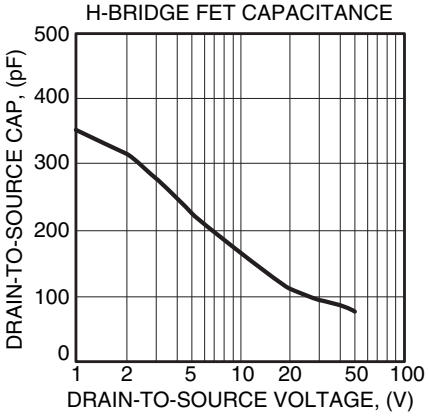
EFFICIENCY CONTOURS



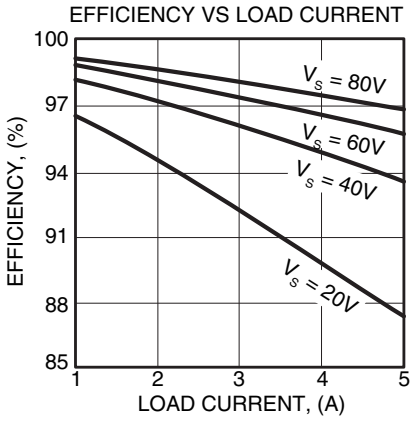
OUTPUT RESISTANCE DRIFT



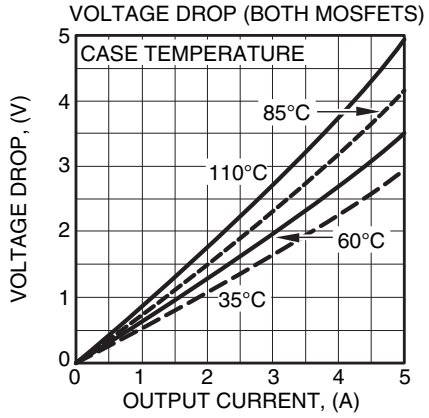
H-BRIDGE FET CAPACITANCE



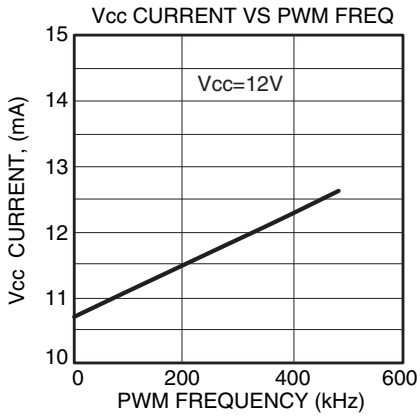
EFFICIENCY VS LOAD CURRENT



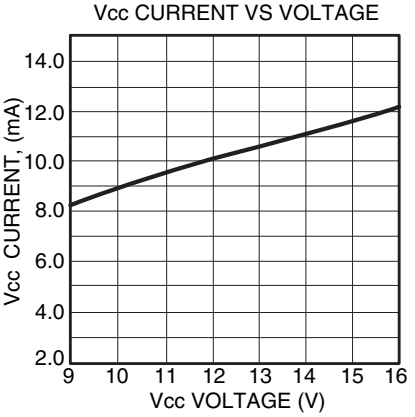
VOLTAGE DROP (BOTH MOSFETS)



Vcc CURRENT VS PWM FREQ



Vcc CURRENT VS VOLTAGE



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

PIN DESCRIPTION

VCC - is the low voltage supply for powering internal logic and drivers for the lowside and highside MOSFETS. The supplies for the highside drivers are derived from this voltage.

V_S - is the higher voltage H-bridge supply. The MOSFETS obtain the output current from this supply pin. The voltage on this pin is limited to +80V by the drive IC. The MOSFETS are rated at 100 volts. Proper by-passing to GND with sufficient capacitance to suppress any voltage transients, and to ensure removing any drooping during switching, should be done as close to the pins on the hybrid as possible.

A OUT - is the output pin for one half of the bridge. When the PWM input is high, this output will be pulled up to Vs.

B OUT - is the output pin for the other half of the bridge. When the PWM input is low, this output will be pulled up to Vs.

RSENSE - This is the common connection for the bottom of the bridge. This can have a sense resistor connected to the Vs return ground for current limit sensing, or can be connected directly to ground. The maximum voltage on this pin is ±2 volts with respect to GND.

GND - is the return connection for the input logic and Vcc.

PWM INPUT - is a TTL compatible input pin for providing the PWM signal to modulate the output switches. The duty cycle can be between 0% (DC low) and 100% (DC high).

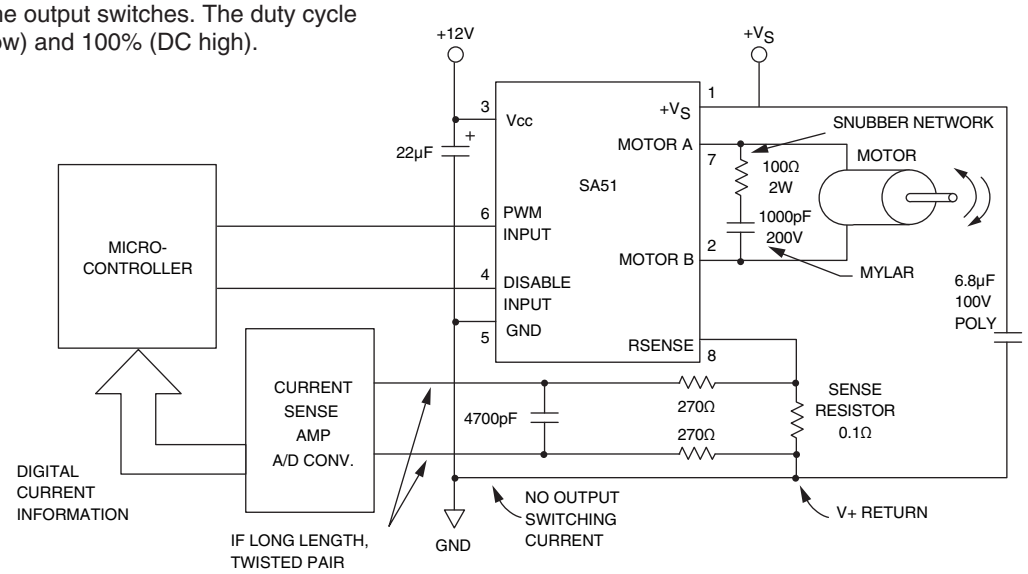
DISABLE INPUT - is a TTL compatible input for providing a shutdown signal to the hybrid for disabling all four switches in the bridge regardless of the PWM input level. A digital 1 disables, a digital 0 enables.

TYPICAL SYSTEM OPERATION

Below is a diagram of a typical application of the SA51. The design Vcc voltage is +12 volts and should have a low ESR bypass capacitor such as a tantalum electrolytic. The PWM and DISABLE signals are typically provided by some type of microprocessor control. The PWM signal will be a TTL signal with a pulse frequency required by the system, and pulse duty cycles according to the required direction/speed. A 0% duty cycle (continuous TTL low) will mean full voltage to the motor in one direction. A 100% duty cycle (continuous TTL high) will mean full voltage to the motor in the other direction. A 50% duty cycle will hold the motor at 0 RPM.

Current sensing is done in this case by a 0.1 ohm sense resistor to sense current from either leg of the bridge. It is important to make the high current traces as wide as possible to keep inductance down. The storage capacitor connected to the +Vs and the hybrid GND should be large enough to provide the high energy pulse without the voltage sagging too far. The storage capacitor should be a low ESR ceramic capacitor or large polypropylene capacitor. Mount capacitor as close to the hybrid as possible. The connection between GND and the +Vs return should not be carrying any motor current. The sense resistor signal is common mode filtered as necessary to feed the limiting circuitry for the microprocessor. This application will allow full four quadrant torque control for a closed loop servo system.

A snubber network is usually required, due to the inductance in the power loop. It is important to design the snubber network to suppress any positive spikes above +V_S and negative spikes below -2V with respect to Pin 5 (GND) of the hybrid.



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